REMARKS

Please reconsider the present application in view of the above amendments and the following remarks. Applicant thanks the Examiner for carefully considering the present application. At the outset, Applicant respectfully requests acknowledgement of the formal drawings filed April 16, 2004. For your convenience, a copy of the formal drawings as filed together with the stamped return postcard indicating receipt by the USPTO is enclosed.

I. Disposition of Claims

Claims 1-3, 5-13, 15, 17, and 18 are pending in this application. By way of this reply, claims 1 and 13 have been amended.

II. Claim Amendments

Claim 1 has been amended to recite that the flip-flop circuit of claim 1 comprises a clock input control stage that provides delayed versions of the clock input and is coupled to the data input control stage and the scan input control stage. No new matter has been added by way of this amendment as support for this amendment may be found, for example, Figure 5 of the present application.

Claim 13 has been amended to recite generating a clock input control stage that provides delayed versions of the clock input to the data input control stage and the scan input control stage. No new matter has been added by way of this amendment as support for this amendment may be found, for example, in Figure 5 of the present application.

The included amendments merely clarify the invention and therefore, will not

require a new search.

III. Rejection(s) under 35 U.S.C § 102

Claims 1-3, 5-13, 15, 17, and 18 of the present application were rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,150,861 issued to Matsunaga et al. (hereinafter "Matsunaga"). For the reasons set forth below, this rejection is respectfully traversed.

Latches and flip-flops are two important logic blocks used in the design of a computer system. Flip-flops, like latches, are memory elements that provide storage for at least one bit, i.e., it can at least store a '1' or a '0.' The present application relates to an improved flip-flop with embedded scanning capabilities. As exemplarily shown in Figure 5 of the present application, the flip-flop **80** contains a data input control stage **123** and a scan input control stage **127** on either end. The use of the embedded scan logic improves the performance of the flip-flop compared to the flip-flops that use separate circuitry for the scan logic.

Additionally, the present invention uses a clock input stage **99** that inputs a clock signal **CLK** and uses inverters **98, 100, 102, 104** to generate delayed versions of the clock signal **CLK**. The various delayed versions of the clock signal are then used to control the operations of the data input control stage **123**, scan input control stage **127**, master stage **82**, and the slave stage **84**. Further, the flip-flop circuit of the present invention utilizes embedded scan logic. Apart from the master stage **82** and the slave stage **84**, no additional latches are used to store the scan input **SI** which is directly connected to the master stage **82** through a sixth NMOS **126**. The use of the embedded

scan logic requires less implementation space and may increase the performance relative to flip-flops with scan circuitry added to flip-flop circuitry.

Accordingly, amended independent claims 1 requires, in part, a clock input control stage that provides delayed versions of the clock input and is *coupled to the data input control stage and the scan input control stage*. Amended independent claim 13 has a corresponding method limitation.

Matsunaga, in contrast to the present invention, fails at least to disclose the limitations of amended independent claims 1 and 13 discussed above. While Matsunaga discloses a flip-flop with embedded scan capabilities, as shown in Figure 2 of Matsunaga, each of the purported master stage **36**, purported slave stage **48**, and purported scan stage **22** are controlled by the same phase of the clock signal **CLK**. The purported data input control stage **34** does not even input a clock signal. Thus, in Matsunaga there is no need for delayed versions of a clock input. Moreover, Matsunaga uses a multiplexer **34** to select the data **D** or scan **SCAN** as the input to the master stage **36**. Therefore, Matsunaga fails to disclose or otherwise teach a flip-flop with a clock input control stage that provides delayed versions of the clock input and is coupled to a data input control stage and a scan input control stage as required by amended independent claims 1 and 13 of the present application.

In view of the above, Matsunaga fails to show or suggest the present invention as recited in amended independent claims 1 and 13 of the present application. Thus, amended independent claims 1 and 13 of the present application are patentable over Matsunaga. Dependent claims are allowable for at least the same reasons. Accordingly, withdrawal of this rejection is respectfully requested.

IV. Conclusion

Applicant believes this reply is fully responsive to all outstanding issues and places this application in condition for allowance. If this belief is incorrect, or other issues arise, the Examiner is encouraged to contact the undersigned or his associates at the telephone number listed below. Please apply any charges not covered, or any credits, to Deposit Account 50-0591 (Reference Number 03226.082001;P5751).

Respectfully submitted,

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